

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2822
JF

Applicant: Leonard Forbes et al.

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Docket No.: 303.324US2

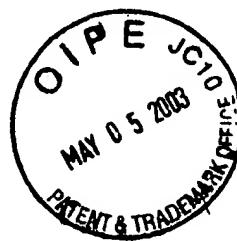
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Examiner: Michael Trinh

Group Art Unit: 2822



Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- A return postcard.
- An Amendment and Response (22 Pages).
- A Supplemental Information Disclosure Statement (1 pg.), Form 1449 (1 pg.), and copies of 10 cited documents.
- A check in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 30th day of April, 2003.

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